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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,144	07/15/2003	Aphrodite Chen	COR 128	6077
7590 RABIN & BERDO, P.C. 1101 14th Street, N.W. Washington, DC 20005		07/02/2007	EXAMINER ZAIDI, SYED	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 07/02/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/619,144

Applicant(s)

CHEN, APHRODITE

Examiner

Syed Zaidi

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 April 2007.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-14 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 15 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Response to Arguments

- Applicant's Amendment filed 4/24/2007 is acknowledged.
- Claims 1-14 are rejected.

Applicant's arguments filed 04/24/2007 have been fully considered but they are not persuasive (page 14-22).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Duvvury (U.S. Patent Application Publication # 2005/0213560 A1) in view of Anderson et al. (U.S. Patent Application Publication # 2003/0217123 A1).

Consider claim 1, Duvvury discloses and shows a single chip Ethernet switch (abstract, [0013] lines 1-2, [0019]) comprising: a physical layer entity (PHY) including a plurality of ports ([0019], line 3-4); an address table for being written to and read out information to operate the plurality of ports ([0020]); a switch for switching the Ethernet switch to a daisy chain test mode ([0075]), but does not clearly disclose an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively.

In the same field of endeavor Anderson et al. clearly show and disclose an address resolution control logic including a test engine for performing a packet source address learning process under the daisy

chain test mode to deliver a test packet through the plurality of ports progressively ([0573]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively as taught by Anderson et al. with the single chip Ethernet switch disclosed by Duvvury for the purpose of fast initialization of an address table and packet source address learning process in an Ethernet switch networking.

Consider claim 2, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch further comprising an input for receiving the test packet ([0076]). This is done by monitoring all input IP packets destined to each switch and checking whether the source IP address of the input packet matches any of the CMP addresses. If there is a match, then conflict is declared. ([0099]).

Consider claim 3, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch further comprising a packet generator for generating the test packet. Data packets are sent between the commander 100 and member switches 102-A-102-N via the network connection. ([0086]).

Consider claim 4, and as applied to claim 3 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch further comprising a register for storing information of the test packet. This method has proven to be satisfactory in field tests. ([0100,0105]). With the commander switch at the center, all of the member switches may be added to the cluster at once. On the other hand, if the switches are connected in a daisy-chain topology, as in FIG. 9, the candidate switch that is connected to the commander switch is added first, and then each subsequent switch in the chain is added as it is discovered by CDP. ([0075]).

Consider claim 5, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch further comprising a verification unit for verifying the test

packet ([0018]) and monitoring logic for monitoring a source IP address of input IP packets received by said member network device. Ethernet switch 200 also includes a frame buffer memory 210, 212, for each port, a source address table memory 220, discovery protocol logic 230, learning logic 240, forwarding logic 250, packet redirection logic 260, and a configuration and management interface 270 as mention figure 2-B ([0019]).

Consider claim 6, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the further comprising an output for sending out the test packet ([0093]) and clearly explain some other IP station can be using the same address as an automatically assigned CMP address. Thus, both the commander switch and the member switches constantly check for conflicts, and in case of a conflict a new CMP address is generated. Duvvury et al further explain in figure 13 is a block diagram illustrating the CMP/RARP packet format according to aspects of the present invention.

Consider claim 7, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch wherein the test engine includes a writing apparatus for writing a set of initial addresses to the address table under the daisy chain test mode ([0067]). Explain when a member switch is added to a cluster, the commander generates a unique cluster IP address and assigns it to the member switch. The commander's cluster IP address is also passed to the member switch. These cluster IP addresses are dynamically assigned. When the commander finds a conflict with one of the assigned cluster IP addresses then the commander resolves the conflict by selecting another cluster IP address when a member switch is added to a cluster, the commander generates a unique cluster IP address and assigns it to the member switch. The commander's cluster IP address is also passed to the member switch. These cluster IP addresses are dynamically assigned. Then the switches that are directly connected to the commander switch may be added first, and then the daisy-chained switches may be added one at a time in a cluster configuration, known as a "daisy chain" configuration, is shown in FIG. 9. ([0067]).

Consider claim 8, and as applied to claim 1 above, Duvvury, as modified by Anderson et al., clearly shows and discloses the switch wherein the packet source address learning process sets a packet destination address as a next port. ([0023]). The total number of ports available for connecting to workstations or other network devices on each LAN switch is diminished due to the dedicated inter switch connections that are necessary to implement the cascaded configuration. The source and destination addresses of Ethernet packets under control of the configuration and management interface 270 and forwards them to other network devices in a cluster configuration. ([0043]).

4. **Claims 9-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chase et al. (U.S. Patent Application Publication # 2004/0202157 A1) in view of Duvvury (U.S. Patent Application Publication # 2005/0213560 A1).

Consider claim 9, Chase et al. disclose and show daisy-chain fashion allowing each MSP to statistically multiplex information onto,

and to statistically de-multiplexing information off the ring infrastructure and such a technique for offering such shared service in a Multi-Protocol Label Switching Network is disclosed in a daisy chain fashion. [A daisy chain test for a single chip Ethernet switch integrated with a physical layer entity including a plurality of ports, the switch having an address table for being written to and read out information to operate the plurality of ports, the test comprising the steps of: connecting each of the plurality of ports to a respective passive loop-back device; selecting a start transmission port and a stop receiving port from the plurality of ports; supplying a test packet to the start transmission port; and proceeding a packet source address learning process for delivering the test packet from the start transmission port to the stop receiving port progressively.], but does not expressly disclose address learning process for delivering the test packet from the start transmission port to the stop receiving port progressively. ([0017]).

In the same field of endeavor, Duvvury discloses clearly shows and discloses the switch wherein the packet source address learning process sets a packet destination address as a next port. ([0023]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate [Chase] with [Duvvury] for the purpose of daisy chain test for a single Chip for Ethernet switch ([0086]).

Consider claim 10, and as applied to claim 9 above, Chase et al., as modified by Duvvury, disclose the test further comprising inputting the test packet to the switch ([0004]). However, some customers may require multi-protocol support, or may otherwise require conventional PVCs so that the traffic streams must be mapped into Frame Relay or ATM PVCs as depicted in FIG. 5, which illustrates a portion of a MAN 10000 having a CO MSP12000.sub.4 serving an ATM switch 30 that receives traffic from the MAN. In an Ethernet protocol network having a plurality of platforms, with at least a first second platforms serving a group of members, a method of routing at least one frame from at least one sending member of group served by a first platform to at least one receiving member of the served by a second platform, comprising the steps of: (a) receiving at said first platform said at least one frame from said sending member;

Consider claim 11, and as applied to claim 9 above, Chase et al., as modified by Duvvury, disclose the test further comprising generating the test packet in the switch ([Abstract]) for Ethernet access to packet-based services. Chase et al clearly explain to packet-bases services, such as ATM, Frame Relay, or IP while advantageously providing a mechanism for assuring security and regulation of customer traffic ([0028]). Upon receipt of each customer-generated information frame (20), an ingress Multi-Service Platform (MSP) (12₂) "tags" the frame with a customer descriptor (22') that specifically identifies the recipient customer. In practice, the MSP tags each frame by overwriting the Virtual Local Area Network (VLAN) identifier (22) with the routing descriptor. Further, the PER 1800 of FIG. 4 also maps the QoS level specified in the customer descriptor in the frame to assure that the appropriate quality of service level is applied to the particular frame ([Abstract]).

Consider claim 12, and as applied to claim 9 above, Chase et al., as modified by Duvvury, disclose the test further comprising verifying the test packet after the stop receiving port ([0006]). Chase et al clearly explain the above-described embodiments merely

illustrate the principles of the invention. Those skilled in the art may make various modifications and changes that will embody the principles of the invention and fall within the spirit and scope thereof.

Descriptor, the PER 1800000 of FIG. 7 routes traffic to a particular one of several different networks, e.g., an Intranet VPN 42.sub.1, a voice network 42.sub.2 and the Internet 42.sub.3, in accordance with the customer descriptor 22' written onto the frame by the MSP 1200000.sub.2. The ATM switch 30 then maps the frame to the appropriate PVC in accordance with the customer descriptor in the frame in a manner similar to the mapping described with respect to (FIG. 3), ([0026]).

Consider claim 13, and as applied to claim 12 above, Chase et al., as modified by Duvvury, disclose the test further comprising sending out the test packet from the stop receiving port ([0026]). Chase et al., clearly Explain In an Ethernet protocol network having a plurality of platforms, with at least a first second platforms serving a group of members, a method of routing at least one frame from at least one sending member of group served by a first platform to at

least one receiving member of the served by a second platform, comprising the steps of: (a) receiving at said first platform said at least one frame from said sending member; (b) modifying said one frame with a customer descriptor that identifies said group of members; (c) mapping the customer descriptor to a path in the network between first and second platforms; and (d) routing the frame on the path to the receiving member served by the second platform. ([0017]). ([0006]).

Consider claim 14, and as applied to claim 9 above, Chase et al., as modified by Duvvury, disclose the test wherein the learning process sets a packet destination address as a next port ([0002]). Chase et al clearly explain that an Ethernet Metropolitan Area Network (10) provides connectivity to one or more customer premises (16.sub.1, 16.sub.2, 16.sub.3) to packet-bases services, ([0006]). Such as ATM, Frame Relay, or IP while advantageously provides a mechanism for assuring security and regulation of customer traffic. Upon receipt of each customer-generated information frame (20), an ingress Multi-Service Platform (MSP) (12₂) "tags" the frame with a customer descriptor (22') that specifically identifies the recipient

customer. In practice, the MSP tags each frame by overwriting the Virtual Local Area Network (VLAN) identifier (22) with the routing descriptor. This invention relates to a technique enabling access to packet-based services, and sets a packet destination address as a next port. ([0004]).

Response to Arguments

- Applicant's Amendment filed 4/24/2007 is acknowledged.
- Claims 1-14 are rejected.

Applicant's arguments filed 04/24/2007 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that **Duvvury** fails to teach “a switch for switching the Ethernet switch to a daisy chain test mode” and “an address resolution control logic including a test engine for performing a packet source addresses learning process under the daisy chain (paragraph 0075 lines 5-10) test mode to deliver a test packet through the plurality of ports progressively”, as recited in the present claim 1.

However examiner respectfully disagree, further more as provided above, **Anderson et al.** teaches module are installed on the daisy chain (paragraph 0036 lines 3-13) and all the modules should be re-verified by the module management software (paragraph 0037 and lines 3-7).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively as taught by **Anderson et al.** with the single chip Ethernet switch disclosed by **Duvvury** for the purpose of fast initialization of an address table and packet source address learning process in an Ethernet switch networking.

Regarding claim 1, Applicant further argues that “an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively”.

However, examiner respectfully disagree, further in the same field of endeavor **Anderson et al.** clearly show and disclose an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain (paragraph 0036, lines 3-13) test mode to deliver a test packet through the plurality of ports progressively (paragraph 0005, lines 3-7).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively as taught by **Anderson et al.** with the single chip Ethernet switch disclosed by **Duvvury.** for the purpose of fast initialization of an address table and packet source address learning process in an fast switch networking.

Regarding claim 1, Applicant further argues that **Anderson's** system perform to accessing and operating personal computer remotely as opposed to Ethernet switch communication.

However, examiner respectfully disagree, further in the same field of endeavor **Anderson et al.** clearly show and disclose an a remote access PC to facilitate communications between a host computer and a remote computer distantly located relative to each other, a remote access process to establish a logical data path between the host computer and the remote computer a switch (paragraph 0062 lines 3-4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an a remote access PC to facilitate communications between a host computer and a remote computer distantly located relative to each other as taught by **Anderson et al.** and a remote access PC to facilitate communications between a host computer and a remote computer distantly located relative to each other with fast switching communication.

Regarding claim 1, Applicant further argues that **Duvvury**. nor **Anderson's** system teaches or suggests " an address resolution control logic including a test engine for performing a packet source

address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively”.

However examiner respectfully disagree, further in the same field of endeavor **Anderson et al.** clearly show and disclose an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively (paragraph 0015 and lines 4-11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate an address resolution control logic including a test engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively as taught by **Anderson et al.** with the single chip Ethernet switch disclosed by **Duvvury.** for the purpose of fast initialization of an address table and packet source address learning process in an Ethernet switch networking.

Regarding claim 9, applicant further argues that **Chase et al.,** fail to teach or suggest “a packet source address learning process for

delivering the test packet from the start transmission port to the stop receiving port progressively” as recited in present claim 9, and proceeding a packet source address learning process for delivering the test packet from the start transmission port to the stop receiving port progressively], but does not expressly disclose address learning process for delivering the test packet from the start transmission port to the stop receiving port progressively.

However examiner respectfully disagree, further in the same field of endeavor, **Duvvury**. discloses clearly shows and discloses the switch wherein the packet source address learning process sets a packet destination address as a next port (paragraph 0023 lines 3-9)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate **(Chase)** with **(Duvvury)** for the purpose of daisy chain test for a single Chip for Ethernet switch.

Regarding claim 9, applicant further argues that **Duvvury**. fail to teach or disclose “a packet source address learning process for delivering the test packet from the start transmission port to the stop receiving port progressively” (paragraph 0014, lines 1-8).

However examiner respectfully disagree, further in the same field of endeavor, **Duvvury**. discloses clearly shows and discloses the switch wherein the packet source address learning process sets a packet destination address as a next port. (paragraph 0022 lines 2-8).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate **(Chase)** with **(Duvvury)** for the purpose of daisy chain test for a single chip for Ethernet switch.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action:

Any response to this Office Action should be **faxed to (571) 273-8300**
or mailed to:

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Hand-delivered responses should be brought to

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Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Syed S.Zaidi whose telephone number is (571) 270-1779. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema S.Rao can be

reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Syed S.Zaidi
S.Z./sz

Seema S. Rao
SEEMA S. RAO 6/25/07
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

June 19, 2007